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09/942,835	08/30/2001	John Robertson Tower	SAR 14108	9999

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,835	TOWER ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,7-11,13-18,20,21,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7-11,13-18,20,21,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal brief

1. In view of the appeal brief filed on 9/19/2005, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.1 13 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claim Objections

2. Claim 20 is objected to because of the following informalities: Claim 20 recites the limitation "the component" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

4. Claims 1, 3, 7-11, 13-15 and 18 and are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of "in response to a bias potential applied to the at least two gate electrodes" as recited in claims 1, 7 and 11are unclear as to what happens in response to applying bias potential to the at least two gate electrodes.

The claimed limitations of "at least two gate electrodes being separated by an inter-electrode gap in the substrate" as recited in claims 1, 11 and 18 are unclear for the following reason. The inter-electrode gap (210), as claimed, is formed between the two electrodes. Thus the inter-electrode gap is separated from the substrate (110) by gate oxide (101, refer to fig. 4A for example). Therefore, it is unclear how the inter-electrode gap can be located in the substrate (110).

The claimed limitations of "apparatus ... selected from a group consisting a semiconductor region" as recited in claims 1, 11 and 18, are unclear as to how a semiconductor region can be an apparatus.

The claimed limitations of "photo-gate optical sensor" as recited in claim 11 and the limitation of "the photo-gate", as recited in dependent claim 13 is unclear if the photo-gate optical sensor and the photo-gate are same element or not.

The claimed limitations of "the further well region forming a further charge barrier well" as recited in claims 9 and 14 are unclear how a well region can form another well region and what does it structurally mean.

The claimed limitations of "the plurality of further diffusion regions forming a charge sink" as recited in claims 9 and 14 are unclear how a plurality of diffusion regions can form one charge sink.

Claim 21 is rejected under 35 U.S.C. 112, second and fourth paragraphs. It is unclear how "an electronic camera system" of claim 21 further limits an imager according to one of claims 18 and 20. This rejection could be overcome if the claim were put in completed form as an independent claim like claim 18 including all the limitation of claims 18 and 20.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 20 is rejected under 35 U.S.C. 102(b) as being anticipated by Tohyama US patent No. 4,875,084.

Tohyama teaches a back Illuminated Imager (fig. 8) comprising: a substrate (21) of a first conductivity type (p) having: a front side and a back side (fig. 8); photodetector (photoelectric converting region 24) formed in the front side of the substrate (upper side of the substrate); a well region (26) of a second conductivity type (n), opposite to the first conductivity type (p), formed in the front side of the substrate and separate from the photodetector (24), the well region and the substrate forming a semiconductor junction (refer to fig. 8); and at least one diffusion region (30) in the well region of the second

conductivity type (n) forming a component of the back illuminated imager; whereby the component of the back illuminated imager is shielded from photocarriers generated in response to photons (35) received at the back side of the substrate by the semiconductor junction (junction between 21 and 26, refer to fig. 8).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

8. Claims 1, 7-11, 13-15, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hynecek US patent No. 4,995,061 in view of Fox, US patent No. 6,465,820.

Regarding claim 1, as best the examiner is able to ascertain the claimed invention Hynecek teaches (fig. 1a) a charge coupled device made on a substrate (10) of a first conductivity type (p), the charge coupled device comprising: a dielectric layer (18) overlaying at least a portion of the substrate (10), and at least two gate electrodes (20, 22) overlaying the dielectric layer (18), the at least two gate electrodes configured to define at least two charge wells (14, 16), the at least two gate electrodes being separated by an inter-electrode gap (the gap between 20 and 22) and apparatus for stabilizing the inter-electrode gap, is a means for applying respective bias potentials (refer to fig. 1a, contacts made to 20 and 22) to the at least two gate electrodes (20 and 22), the bias potential being sufficient to cause a fringing field to extend across the inter-

electrode gap from at least on of the at least two gate electrodes (20 or 22). Since Hynecek teaches a means for applying respective bias potentials to the at least two gate electrodes, the structure of Hynecek is inherently capable providing a means for stabilizing the inter-electrode gap, by applying respective bias potentials to the at least two gate electrodes.

Hynecek does not explicitly state that the dielectric layer overlaying portion of the substrate is a CMOS gate dielectric layer.

Fox teaches forming a charge transfer device (CCD) that is compatible with CMOS sensor for better integration with CMOS processing (col. 9, lines 52-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dielectric layer of Hynecek as a CMOS dielectric layer as taught by Fox, in order in order to reduce the processing step of making the device and in order to use the device in an application which requires CMOS imaging sensor.

The recitation of "a charge coupled device made according to a standard CMOS process" is not given patentable weight because it is considered a product-by-process claim. It is the patentability of the claimed product and not of recited process steps, which must be established. Therefore, when the prior art discloses a product, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and

particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim is "product by process" claim or not. Furthermore the combined structure of Hynecek and Fox results in a charge coupled device made according to a standard CMOS process (refer to col. 1, lines 10-14, Fox).

Regarding claim 7, as best the examiner is able to ascertain the claimed invention Hynecek teaches (fig. 1a) substantially the entire claimed structure of claim 1 above in including a charge coupled device comprising: a dielectric layer (18) overlaying at least a portion of the substrate (10), at least two gate electrodes (20, 22) overlaying the dielectric layer (18), the at least two gate electrodes configured to define at least two charge wells (14, 16), the at least two gate electrodes being separated by an inter-electrode gap (the gap between 20 and 22) and apparatus for stabilizing the inter-electrode gap, is a means for applying respective bias potentials (refer to fig. 1a, contacts made to 20 and 22) to the at least two gate electrodes (20 and 22), the bias potential being sufficient to cause a fringing field to extend across the inter-electrode gap from at least on of the at least two gate electrodes (20 or 22). Since Hynecek teaches a means for applying respective bias potentials to the at least two gate electrodes, the structure of Hynecek is inherently capable providing a means for

stabilizing the inter-electrode gap, by applying respective bias potentials to the at least two gate electrodes.

Regarding claim 8, Hynecek teaches substantially the entire claimed structure of claim 1 above including form a photo-gate optical sensor (CCD imager) and the charge coupled device further comprises: a well region of a first conductivity type (24,n), adjacent to the photo-gate for forming a charge barrier well, the charge bather well being configured to divert photo-carriers into at least the photo-gate; and a diffusion region (23) of a second conductivity type (p), different from the first conductivity type, the diffusion region being formed inside the charge barrier well 24, refer to fig. 1a) and being configured as an anti-blooming drain. Since Hynecek teaches the same structure as the claimed invention, the charge barrier well is inherently capable of being configured as an anti-blooming drain.

Regarding claim 9, Hynecek teaches substantially the entire claimed structure of claim 1 above including a further well region (26) of the first conductivity type (n), the further well region forming a further charge barrier well; and a plurality of further diffusion regions (23) of the second conductivity type (p) in the further charge barrier well, the plurality of further diffusion regions (23) forming a charge sink.

Regarding claim 10, Hynecek teaches substantially the entire claimed structure of claim 1 above including a plurality of transistors include a reset transistor and an emitter follower amplifier both coupled to the charge sink (fig. 1a and 4).

Regarding claim 32, Hynecek teaches (fig. 1a) substantially the entire claimed structure of claim 1 above including the at least two gate electrodes include polysilicon gate electrodes (column, 4, lines 39-41).

Regarding claim 11, as best the examiner is able to ascertain the claimed invention, Hynecek teaches substantially the entire claimed structure of claim 1 above including a charge coupled device (CCD) array (col. 4, lines 18-24), the array being formed of a plurality of single polysilicon CMOS pixels, each pixel including, a first dielectric layer (12) overlaying the substrate.

The recitation "an optical sensor circuit for receiving photocarriers from a source" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claims 13-15, Hynecek teaches substantially the entire claimed structure of claims 8-10 and 11 above including a well region (24) of the first conductivity type (n), adjacent to the photogate for forming a charge barrier well, the charge barrier well being configured to divert photo-carriers into at least the photogate; and a diffusion region (23) of a second conductivity type (p), different from the first conductivity type, the diffusion region being formed inside the charge barrier well and

being configured as an anti-blooming drain. Since Hynecek teaches the same structure as the claimed invention, the charge barrier well is inherently capable of being configured as an anti-blooming drain.

Regarding claim 31, Hynecek teaches (fig. 1a) substantially the entire claimed structure of claim 11 above including wherein the semiconductor layer is a transmission channel region and the transmission channel is a CMOS n-well (the combined structure of Hynecek and Fox teach a CCD structure that is compatible with CMOS process).

9. Claims 3, is rejected under 35 U.S.C. 103(a) as being unpatentable over Hynecek, Fox and in view of Ohsawa et al. US patent No. 5,210,433.

Regarding claim 3, Hynecek teaches substantially the entire claimed structure of claim 1 above except explicitly stating that a further dielectric layer formed over the at least two gate electrodes; and a further gate electrode formed overlying the further dielectric layer and positioned over the inter-electrode gap.

Ohsawa teaches (fig. 16) forming dielectric layer (122) over at least two gate electrodes (130a and 130b) and forming a further electrode (132) overlying the further dielectric layer (122) and positioned over the inter-electrode gap (Gv) in order to form an improved solid state imaging device which is highly integrated and much superior in signal charge transfer efficiency (col. 1, lines 55-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the further dielectric layer and the further electrode taught by Ohsawa in the structure of Hynecek in order in order to form an improved

solid state imaging device which is highly integrated and much superior in signal charge transfer efficiency.

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fuji, US patent No., 4,952,523 in view of Fox.

Fuji teaches a substrate (10) of a first conductivity type (p); a well region (32) of a second conductivity type (n), opposite to the first conductivity type (p); an oxide layer (12) formed over the least the well region (32); first (42) and second (44) electrodes are formed of polysilicon gate electrodes formed on the oxide layer (12) (col. 7, lines 54-70) and the first (42) and second (44) gate electrodes being separated by an inter-electrode gap (gap between 42 and 44), wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a buried channel CCD register (col. 8, lines 32-45) and means for applying respective bias potentials to the at least two gate electrodes, the bias potential being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes. Since Fuji teaches a means for applying respective bias potentials to the at least two gate electrodes, the structure of Fuji is inherently capable providing a means for stabilizing the inter-electrode gap, by applying respective bias potentials to the at least two gate electrodes.

Fuji does not explicitly state that the dielectric layer overlaying at least a portion of the substrate is a CMOS gate dielectric layer.

Fox teaches forming a charge transfer device (CCD) that is compatible with CMOS sensor for better integration with CMOS processing (col. 9, lines 52-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dielectric layer of Hynecek as a CMOS dielectric layer as taught by Fox, in order in order to reduce the processing step of making the device and in order to use the device in an application which requires CMOS imaging sensor.

The recitation of "a charge coupled device made according to a standard CMOS process" is not given patentable weight because it is considered a product-by-process claim. It is the patentability of the claimed product and not of recited process steps, which must be established. Therefore, when the prior art discloses a product, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim is "product by process" claim or not. Furthermore the combined structure of Hynecek and Fox results

in a charge coupled device made according to a standard CMOS process (refer to col. 1, lines 10-14, Fox).

11. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda US patent No. 6,088,057 in view of Fujii.

Regarding claims 16 and 17, Hieda teaches (fig. 1) a single monolithic integrated circuit including CCD imager (2) (fig. 1) and a CMOS analog to digital converter (3) coupled to receive image signals from the CCD optical integration section (fig. 1).

Hieda does not explicitly teach an array of CCD imager.

Fujii teaches forming an array of CCD imagers as illustrated in figs. 8 and 9.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an array of CCD imager as taught by Fujii in the structure of Hieda in order to form an imaging device with reduced dark current.

The recitation "a camera system" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

12. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tohyama in view of Savoye US patent No. 6,489,992.

Regarding claim 21, Tohyama teaches substantially the entire claimed structure of claim 20 above except explicitly stating that optics that are configured to focus radiation onto the imager.

Savoye teaches optics (lens) that is configured to focus radiation onto the imager (col. 28, lines 29-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the optics (lens) that is configured to focus radiation onto the imager as taught by Savoye in the structure of Tohyama in order to provide an imaging system that attains superior performance at real time speeds (col. 3, lines 29-34).

The recitation "an electronic camera system" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Response to Arguments

13. Applicant's arguments with respect to claims 1,3, 7-11, 13-15 and 18 have been considered but are moot in view of the new ground(s) of rejection. In response to

applicant's argument that the examiner's conclusion of obviousness with regards to claim 16 and 17 is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D-F are cited as being related CCD imaging device. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
October 2, 2006

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